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Docket No. AMAT/1931

CERTIFICATION UNDER 37 CFR 1.10
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B. Todd Patterson
Signature

Box Patent Application
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Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of:

Inventor(s): **FUSEN CHEN, LIANG-YUH CHEN, RODERICK CRAIG MOSELY, and MOSHE EIZENBERG**

For: **RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION**

Enclosed are:

- [X] Specification, Claims and Abstract (17 pages)
- [X] 10 Sheets of informal Drawings
- [X] Combined Declaration and Power of Attorney
- [ ] Information Disclosure Statement (37 CFR 1.98)
- [ ] Art Cited by Applicant (Form PTO-1449)
- [X] Assignment of Invention to Applied Materials, Inc.
- [X] Recordation Cover Sheet (Form PTO-1595) **(in duplicate)**

The **large-entity** filing fee has been calculated as shown below:

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BASIC FEE				770.00
TOTAL CLAIMS	20	20	x 22 =	
INDEP. CLAIMS	3	3	x 80 =	
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Respectfully submitted,

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UNITED STATES PATENT APPLICATION

FOR

RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION

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RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION

Field of the Invention

The present invention relates to a deposition sequence and related hardware for manufacturing a plug and line typical of a dual damascene structure utilizing a thin conformal barrier layer formed on the via walls.

Background of the Invention

Modern semiconductor integrated circuits usually involve multiple layers separated by dielectric (insulating) layers, such as silicon dioxide or silica, often referred to simply as an oxide layer, although other materials are being considered for use as the dielectric. The layers are electrically interconnected by holes penetrating the intervening oxide layer which contact some underlying conductive feature. After the holes are etched, they are filled with a metal, typically aluminum (however the trend now is to move towards copper) to electrically connect the bottom layer with the top layer. The generic structure is referred to as a plug. If the plug is connected to silicon or polysilicon, the plug is a contact. If the plug is connected to a metal, the plug is a via.

Plugs have presented an increasingly difficult problem as integrated circuits are formed with an increasing density of circuit elements because the feature sizes have continued to shrink. For logic applications, the thickness of the oxide layer seems to be constrained to the neighborhood of 1μm, while the diameter of the plug is being reduced from the neighborhood of 0.25μm or 0.35μm to 0.18μm and below. As a result, the aspect ratios (the ratio of the depth to the minimum lateral dimension) of the plugs are being pushed to 5:1 and above.

As sizes continue to decrease, the characteristics of the material forming the plugs become increasingly important. The smaller the plug, the less resistive the material forming the plug should be for speed performance. Copper is a material which is becoming more important as a result.

Copper has a resistivity of 1.7 $\mu\Omega$.cm. Copper has a small RC time constant thereby increasing the speed of a device formed thereof. In addition, copper exhibits improved reliability over aluminum in that copper has excellent electromigration resistance and can drive more current in the lines.

One problem with the use of copper is that copper diffuses into silicon dioxide, silicon and other dielectric materials. Therefore, barrier layers become increasingly important to prevent copper from diffusing into the dielectric and compromising the integrity of the device. Barrier layers for copper applications are available for inter-dielectric applications. The use of a thin silicon nitride (SiN) layer on the interlayer dielectric will effectively inhibit interlayer diffusion. Within the same dielectric layer it is difficult to provide an effective barrier to prevent leakage between lines. Several technologies are presently under investigation which add a barrier liner to the via sidewall separating the copper metal from the interlayer dielectric. Common physical vapor deposition (PVD) technologies are limited in high aspect and re-entrant structures due to the directional nature of their deposition. The barrier thickness will depend directly upon the structure architecture with the barrier becoming thinner on the sidewall near the structure bottom. Under overhangs on re-entrant structures the barrier thickness, and therefore the barrier integrity, will be compromised.

In contrast, CVD deposited films are by their nature conformal in re-entrant structures. Further, CVD deposited films maintain a high degree of conformity to the structure's lower interface. Silicon nitride (Si_xN_y) and titanium nitride (TiN) prepared by decomposition of an organic material (TDMAT) are common semiconductor manufacturing materials which display the described conformal performance. Both materials are perceived as being good barriers to Cu interdiffusion, but are considered unattractive due to their high resistivity. The high resistive nature of the material would detrimentally effect the via resistance performance which must be maintained as low as possible to maximize logic device performance. Ideally, good barrier would line the sidewalls of the plug shown in Figure 1.

Therefore, there is a need for a process sequence and related hardware which provides a good barrier layer on the via sidewall, but which does not negatively affect the resistance of the plug.

Summary of the Invention

The present invention generally provides a process sequence and related hardware for filling a hole on a substrate with copper. The sequence comprises first forming a reliable barrier layer in the hole to prevent diffusion of the copper into the dielectric layer through which the hole is formed.

One embodiment of the present invention comprises forming a generally conformal barrier layer over a patterned dielectric, etching the bottom of the hole, depositing a second barrier, and then filling the hole with copper. An alternative sequence comprises depositing a first barrier layer over a blanket dielectric layer, forming a hole through both the barrier layer and the dielectric layer, depositing a generally conformal second barrier layer in the hole, removing the barrier layer from the bottom of the hole, and selectively filling the hole with copper.

Brief Description of the Drawings

So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

Figure 1 is a prior art drawing showing a plug filled with copper having a good barrier layer formed on the sidewalls of the plug;

Figures 2-5 show a partial cross-sectional view of a substrate having one process sequence of the present invention performed thereon;

Figure 6 is a flow diagram of one process sequence of the present invention;

Figures 7-12 show a partial cross-sectional view of a substrate having another process

sequence of the present invention performed thereon;

Figure 13 is a flow diagram of another process sequence of the present invention;

Figure 14 is a schematic of a multichamber processing apparatus;

Figure 15 is a cross-sectional view of a high density PVD process chamber;

Figure 16 is a cross-sectional view of a high density CVD process chamber; and

Figure 17 is a cross-sectional flow diagram of a computer controlled processing apparatus.

Detailed Description of a Preferred Embodiment

The present invention provides a process sequence and related hardware to form a copper (Cu) plug having a reliable barrier formed on the sidewall of the plug to prevent Cu diffusion into the dielectric layer through which the plug is formed. In one aspect of the invention, a sequence and related hardware are provided to form a copper plug by first depositing a generally conformal barrier layer, such as Si_xN_y, over a substrate having a plug formed in a dielectric layer deposited thereon. The substrate is then subjected to a pre-clean or other etch process to remove the barrier layer formed at the bottom of the plug at the interface with the underlying layer, typically a metal layer or a silicon or polisilicon layer. A second barrier layer, such as a Ta, TaN, TiSiN or TaSiN layer, is then deposited over the first barrier layer to provide good bottom coverage in the plug and also to cover the corners of the plug where the dielectric layer may have been exposed by the etching process. Copper is then deposited using a high density physical vapor deposition process followed by heated Cu planarization and high pressure fill, chemical vapor deposition or a combination of chemical vapor deposition followed by physical vapor deposition.

In another aspect of the invention, a barrier layer, such as amorphous Si_xN_y, is deposited on a substrate having a blanket dielectric layer, such as SiO_2, formed thereon. The substrate is then patterned to open a plug through both the barrier layer and the dielectric layer to expose the underlying layer. A conformal barrier layer is then formed over the patterned substrate surface including the sidewalls of the plug. The substrate is then subjected to a pre-clean or other etch

process to remove the barrier layer formed on the bottom of the plug at the interface with the underlying layer. Where the underlying layer is a nucleating material, such as Cu or other metal, Cu can be grown selectively within the plug using chemical vapor deposition techniques. Alternatively, the IMP Cu process and pressure fill described above can be used to fill the plug.

Figures 2-6 illustrates and describe one process sequence of the present invention and will be described below. Figure 2 is a partial cross sectional view of a substrate having a plug 20 formed thereon through a dielectric layer 12 to an underlying metal layer 14. A conformal Si_xN_y barrier layer 16 is formed over the patterned surface by CVD techniques to form a generally conformal barrier layer on the sidewalls 18 and bottom of the plug 20. Next, the substrate is exposed to a pre-clean or other etching process to remove the portion of the Si_xN_y layer 22 formed on the bottom of the plug 20 at the interface with the underlying metal layer 14 as shown in Figure 3. Typically, the etching process also removes material at the upper corners of the plug 20 which may expose a portion of the dielectric layer 12. In addition, the deposition on the sidewalls of the plugs tends to be thinner at the bottom than at the top. Accordingly, a second barrier layer 24, such as Ta, TaN, TiSiN and/or TaSiN is sputter deposited using a high density plasma process, such as an ion metal plasma process, (commonly referred to by applicant as an IMP^{tm} process) onto the Si_xN_y layer and exposed dielectric layer 12 as shown in Figure 4. Copper is then deposited using an IMP process followed by a warm Cu planarization and high pressure fill as shown in Figure 5, or deposited using chemical vapor deposition techniques or a combination of chemical vapor deposition techniques followed by physical vapor deposition techniques. Other Cu deposition techniques which are known to fill small features, such as electroplating, can also be used and are within the scope of the present invention. The process sequence is summarized in the flow diagram present in Figure 6.

Figures 7-12 illustrate and describe another process sequence of the present invention and will be described below. Figure 7 shows a blanket dielectric layer 12 formed on a substrate having a barrier layer 15, such as an Si_xN_y layer, formed thereon. In the sequence, a barrier layer 16, such as a Si_xN_y layer, is first deposited on the dielectric layer 12. The substrate is then patterned and

etched to form a plug 20 through the barrier layers 15, 16 and the dielectric layer 12 as shown in Figure 8. Next, a second conformal barrier layer 30 (Si_xN_y) is formed over the patterned surface as shown in Figure 9. The substrate is then exposed to a pre-clean or other etch process to remove the portion of the Si_xN_y layer 30 formed on the bottom of the plug 20 at the interface with the underlying layer as shown in Figure 10. Next, Cu can be selectively grown in the plug in those applications where the underlying layer is a conductive layer which can nucleate CVD of Cu. Additionally, Cu can be sputter deposited in the plug or Cu can be deposited using electroplating to complete the fill of the plug. Thereafter, the substrate can undergo chemical mechanical polishing to remove the excess and unwanted material from the substrate and complete the formation of the desired feature as shown in Figure 12. Figure 13 is a flow diagram which summarizes the process sequence described above.

A schematic of a multichamber processing apparatus 35 suitable for performing the CVD processes of the present invention is illustrated in Figure 14. The apparatus is an "ENDURA" system commercially available from Applied Materials, Santa Clara, California. The particular embodiment of the apparatus 35 shown herein is suitable for processing planar substrates, such as semiconductor substrates, and is provided to illustrate the invention, and should not be used to limit the scope of the invention. The apparatus 35 typically comprises a cluster of interconnected process chambers, for example, CVD and PVD deposition and rapid thermal annealing chambers.

In the context of contact hole filling, a high-density plasma is defined in one sense as one substantially filling the entire volume it is in and having an average ion density of greater than $10^{11}cm^{-3}$ in the principal part of the plasma. The conventional plasma-enhanced PVD reactor produces a plasma of significantly lower ion density. Although high-density plasmas are available in a number of different types of reactors, they are preferably obtained in inductively coupled plasma reactors, such as the type shown in schematical cross-section in Figure 15. For reasons to be described shortly, this is referred to an ionized metal plasma (IMP) reactor.

As shown in this figure, which is meant only to be schematical, a vacuum chamber 40 is

defined principally by a chamber wall 42 and a target backing plate 44. A PVD target 46 is attached to the target backing plate 44 and has a composition comprising at least part of the material being sputter deposited. For the deposition of both tantalum (Ta) and tantalum nitride (TaN), the target 46 is made of tantalum. A substrate 48 being sputter deposited with a layer of a PVD film is supported on a pedestal electrode 50 in opposition to the target 46. Processing gas is supplied to the chamber 40 from gas sources 52, 54 as metered by respective mass flow controllers 56, 58, and a vacuum pump system 60 maintains the chamber 40 at the desired low pressure.

An inductive coil 62 is wrapped around the space between the target 46 and the pedestal 50. Three independent power supplies are used in this type of inductively coupled sputtering chamber. A DC power supply 64 negatively biases the target 46 with respect to the pedestal 50. An RF power source 66 supplies electrical power in the megahertz range to the inductive coil 62. The DC voltage applied between the target 46 and the substrate 48 causes the processing gas supplied to the chamber to discharge and form a plasma. The RF coil power inductively coupled into the chamber 40 by the coil 62 increases the density of the plasma, that is, increases the density of ionized particles. Magnets 58 disposed behind the target 46 significantly increase the density of the plasma adjacent to the target 46 in order to increase the sputtering efficiency. Another RF power source 70 applies electrical power in the frequency range of 100KHz to a few megahertz to the pedestal 50 in order to bias it with respect to the plasma.

Argon from the gas source 54 is the principal sputtering gas. It ionizes in the plasma, and its positively charged ions are attracted to the negatively biased target 46 with enough energy that the ions sputter particles from the target 46, that is, target atoms or multi-atom particles are dislodged from the target. The sputtered particles travel primarily along ballistic paths, and some of them strike the substrate 48 to deposit upon the substrate as a film of the target material. If the target 46 is tantalum and assuming no further reactions, a tantalum film is thus sputter deposited, or in the case of an aluminum target, an aluminum film is formed.

The apparatus also comprises a CVD deposition chamber 40 (shown in Figure 16) having

surrounding sidewalls 45 and a ceiling 50. The chamber 40 comprises a process gas distributor 55 for delivering process gases into the chamber. Mass flow controllers and air operated valves are used to control the flow of process gases into the deposition chamber 40. The gas distributor 55 is typically mounted above the substrate (as shown), or peripherally about the substrate (not shown). A support 65 is provided for supporting the substrate in the deposition chamber 40. The substrate is introduced into the chamber 40 through a substrate loading inlet in the sidewall 45 of the chamber 40 and placed on the support 65. The support 65 can be lifted or lowered by support lift bellows 70 so that the gap between the substrate and gas distributor 55 can be adjusted. A lift finger assembly 75 comprising lift fingers that are inserted through holes in the support 65 can be used to lift and lower the substrate onto the support to facilitate transport of the substrate into and out of the chamber 40. A thermal heater 80 is then provided in the chamber to rapidly heat the substrate. Rapid heating and cooling of the substrate is preferred to increase processing throughput, and to allow rapid cycling between successive processes operated at different temperatures within the same chamber 65. The temperature of the substrate is generally estimated from the temperature of the support 65.

The substrate is processed in a process zone 95 above a horizontal perforated barrier plate 105. The barrier plate 105 has exhaust holes 110 which are in fluid communication with an exhaust system 115 for exhausting spent process gases from the chamber 40. A typical exhaust system 115 comprises a rotary vane vacuum pump (not shown) capable of achieving a minimum vacuum of about 10 mTorr, and optionally a scrubber system for scrubbing byproduct gases. The pressure in the chamber 40 is sensed at the side of the substrate and is controlled by adjusting a throttle valve in the exhaust system 115.

A plasma generator 116 is provided for generating a plasma in the process zone 95 of the chamber 40 for plasma enhanced chemical vapor deposition processes. The plasma generator 116 can generate a plasma (i) inductively by applying an RF current to an inductor coil encircling the deposition chamber (not shown), (ii) capacitively by applying an RF current to process electrodes in the chamber, or (iii) both inductively and capacitively while the chamber wall or other electrode

is grounded. A DC or RF current at a power level of from about 750 Watts to about 2000 Watts can be applied to an inductor coil (not shown) to inductively couple energy into the deposition chamber to generate a plasma in the process zone 95. When an RF current is used, the frequency of the RF current is typically from about 400 KHz to about 16 MHZ, and more typically about 13.56 MHZ Optionally, a gas containment or plasma focus ring (not shown), typically made of aluminum oxide or quartz, can be used to contain the flow of process gas or plasma around the substrate.

A pre-clean chamber which can be used to remove the barrier layer from the bottom of the plug is available from Applied Materials, Inc. of Santa Clara, California. Additionally, other etch chambers known in the field could be used to remove the barrier layer as described.

The process can be implemented using a computer program product 141 that runs on a conventional computer system comprising a central processor unit (CPU) interconnected to a memory system with peripheral control components, such as for example a 68400 microprocessor, commercially available from Synenergy Microsystems, California. The computer program code can be written in any conventional computer readable programming language such as for example 68000 assembly language, C, C++, or Pascal. Suitable program code is entered into a single file, or multiple files, using a conventional text editor, and stored or embodied in a computer usable medium, such as a memory system of the computer. If the entered code text is in a high level language, the code is compiled, and the resultant compiler code is then linked with an object code of precompiled windows library routines. To execute the linked compiled object code, the system user invokes the object code, causing the computer system to load the code in memory, from which the CPU reads and executes the code to perform the tasks identified in the program.

Figure 17 shows an illustrative block diagram of the hierarchical control structure of the computer program 141. A user enters a process set and process chamber number into a process selector subroutine 142. The process sets are predetermined sets of process parameters necessary to carry out specified processes in a specific process chamber, and are identified by predefined set numbers. The process set the desired process chamber, and (ii) the desired set of process parameters

needed to operate the process chamber for performing a particular process. The process parameters relate to process conditions such as, for example, process gas composition and flow rates, temperature, pressure, plasma conditions such as RF and DC bias power levels and magnetic field power levels, cooling gas pressure, and chamber wall temperature.

A process sequencer subroutine 143 comprises program code for accepting the identified process chamber and set of process parameters from the process selector subroutine 142, and for controlling operation of the various process chambers. Multiple users can enter process set numbers and process chamber numbers, or a user can enter multiple process set numbers and process chamber numbers, so the sequencer subroutine 143 operates to schedule the selected processes in the desired sequence. Preferably the sequencer subroutine 143 includes a program code to perform the steps of (i) monitoring the operation of the process chambers to determine if the chambers are being used, (ii) determining what processes are being carried out in the chambers being used, and (iii) executing the desired process based on availability of a process chamber and type of process to be carried out. Conventional methods of monitoring the process chambers can be used, such as polling. When scheduling which process is to be executed, the sequencer subroutine 143 can be designed to take into consideration the present condition of the process chamber being used in comparison with the desired process conditions for a selected process, or the "age" of each particular user entered request, or any other relevant factor a system programmer desires to include for determining scheduling priorities.

Once the sequencer subroutine 143 determines which process chamber and process set combination is going to be executed next, the sequencer subroutine 143 causes execution of the process set by passing the particular process set parameters to the chamber manager subroutines 144a-c which control multiple processing tasks in different process chambers according to the process set determined by the sequencer subroutine 143. For example, the chamber manager subroutine 144a comprises program code for controlling CVD process operations, within the described process chamber 40. The chamber manager subroutine 144 also controls execution of

various chamber component subroutines or program code modules, which control operation of the chamber components necessary to carry out the selected process set. Examples of chamber component subroutines are substrate positioning subroutine 145, process gas control subroutine 146, pressure control subroutine 147, heater control subroutine 148, and plasma control subroutine 149. These different subroutines function as seeding program code means for (i) heating the substrate to temperatures T_S within a range of temperatures ΔT_S, and (ii) introducing a reaction gases into the process zone to deposit a substantially continuous insulating layer on the field portions of the substrate; and deposition growth program code means for (i) maintaining the substrate at a deposition temperatures T_d within a range of temperature ΔT_d, and (ii) introducing deposition gas into the process zone to form an epitaxial growth layer that is grown in the contact holes or vias. Those having ordinary skill in the art would readily recognize that other chamber control subroutines can be included depending on what processes are desired to be performed in the process chamber 40.

In operation, the chamber manager subroutine 144a selectively schedules or calls the process component subroutines in accordance within the particular process set being executed. The chamber manager subroutine 144a schedules the process component subroutines similarly to how the sequencer subroutine 143 schedules which process chamber 40 and process set is to be executed next. Typically, the chamber manager subroutine 144a includes steps of monitoring the various chamber components, determining which components need to be operated based on the process parameters for the process set to be executed, and causing execution of a chamber component subroutine responsive to the monitoring and determining steps.

Example 1

In one example, a process according to the present invention was performed on a wafer having a 0.25 μ via with about a 4:1 aspect ratio. The patterned wafer was first introduced into a

CVD chamber where about 50 Å to about 100 Å of Si_xN_y was deposited on the wafer using CVD techniques. The wafer was then moved into a Pre-clean II chamber where the wafer was subjected to an argon/hydrogen etching environment for about 20 seconds. RF/DC powers of about 300/300W were used. Next, the wafer was moved into an IMP chamber where about 400 Å of TaN was deposited on the wafer. Next, the wafer was introduced into a CVD chamber where about 400 Å of CVD Cu was deposited on the wafer as a wetting layer. Then, Cu was sputtered onto the wafer to complete the fill of the via.

Example 2

In another example, a another process sequence of the present invention was performed on a wafer having a metal 1 feature, a barrier layer and a dielectric layer formed thereon. The wafer was first patterned and etched to form a via connecting the metal 1 feature. Next, the wafer was introduced into a CVD chamber where about 50 Å to about 100 Å of Si_xN_y was deposited on the wafer using CVD techniques. The wafer was then moved into a Pre-clean II chamber where the wafer was subjected to an argon/hydrogen etching environment for about 20 seconds. RF/DC powers of about 300/300W were used. Next, the wafer was introduced into a CVD chamber where the via was selectively filled with Cu.

While the foregoing is directed to the preferred embodiment of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims which follow.

Claims:

1. A method of filling a hole through a dielectric layer in an integrated circuit, comprising:

a) depositing a generally conformal first barrier layer in the hole;

b) removing the first barrier layer formed on the bottom of the hole;

c) sputter depositing a second barrier layer under conditions of a high density plasma; and

d) depositing a metal layer in the hole.

2. The method of claim 1 wherein the first barrier layer is deposited using chemical vapor deposition techniques.

3. The method of claim 2 wherein the barrier layer is comprised of Si_xN_y.

4. The method of claim 3 wherein a portion of the first barrier layer formed on the bottom of the hole is removed using etching techniques.

5. The method of claim 4 wherein the metal layer deposited in the hole is copper.

6. The method of claim 5 wherein the metal layer is deposited using chemical vapor deposition techniques.

7. The method of claim 5 wherein the metal layer is deposited using physical vapor deposition techniques.

8. The method of claim 1 wherein the first barrier layer comprises Si_xN_y.

9. The method of claim 8 wherein the second barrier layer comprises a material selected from the group consisting of Ta, TaN, TaSiN, TiSiN and combinations thereof.

10. The method of claim 9 wherein the metal layer sputter deposited in the hole is copper.

11. The method of claim 10 wherein the second barrier layer is sputter deposited under the conditions of a high density plasma.

12. The method of claim 11 wherein the metal is sputter deposited under the conditions of a high density plasma.

13. The method of claim 12 wherein the metal is heated to a temperature of between about room temperature and about 500°C and then subjected to a pressurized environment.

14. The method of claim 13 wherein the pressurized environment is in the range of about 1000 psi to about 100,000 psi.

15. A method of filling a hole through a dielectric layer in an integrated circuit, comprising:

a) depositing a first barrier layer over a blanket dielectric layer;

b) forming a hole through the barrier layer and the dielectric layer to expose an underlayer;

c) depositing a second generally conformal barrier layer in the hole;

d) removing the barrier layer formed at the bottom of the hole;

e) selectively depositing a metal layer in the hole.

16. The method of claim 15 wherein the first barrier and second barrier layers are comprised of

Si_xN_y.

17. The method of claim 16 wherein the first and second barrier layers are formed using chemical vapor deposition techniques.

18. The method of claim 17 wherein the barrier layer formed on the bottom of the hole is removed by sputter etching techniques.

19. An integrated processing tool, comprising:

a central transfer chamber having a robot assembly disposed at least partially therein for moving substrates;

a chemical vapor deposition chamber for depositing Si_xN_y;

a high density plasma physical vapor deposition chamber connected to the transfer chamber having a target comprising tantalum;

an etch chamber capable of achieving a high density plasma; and

a high density plasma physical vapor deposition chamber connected to the transfer chamber having a target comprising copper.

20. The method of claim 5 wherein the metal layer is deposited by first depositing a wetting layer using chemical vapor deposition techniques and then filling the hole using physical vapor deposition techniques.

Abstract of the Disclosure

The present invention provides a process sequence and related hardware for filling a hole with copper. The sequence comprises first forming a reliable barrier layer in the hole to prevent diffusion of the copper into the dielectric layer through which the hole is formed. One sequence comprises forming a generally conformal barrier layer over a patterned dielectric, etching the bottom of the hole, depositing a second barrier, and then filling the hole with copper. An alternative sequence comprises depositing a first barrier layer over a blanket dielectric layer, forming a hole through both the barrier layer and the dielectric layer, depositing a generally conformal second barrier layer in the hole, removing the barrier layer from the bottom of the hole, and selectively filling the hole with copper.

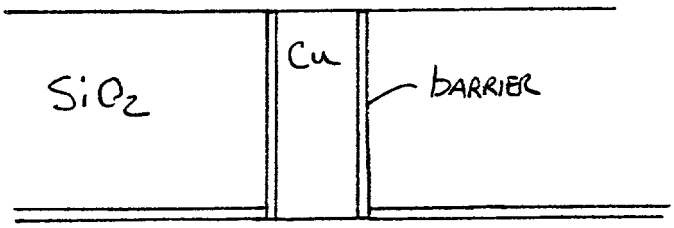

FIGURE 1

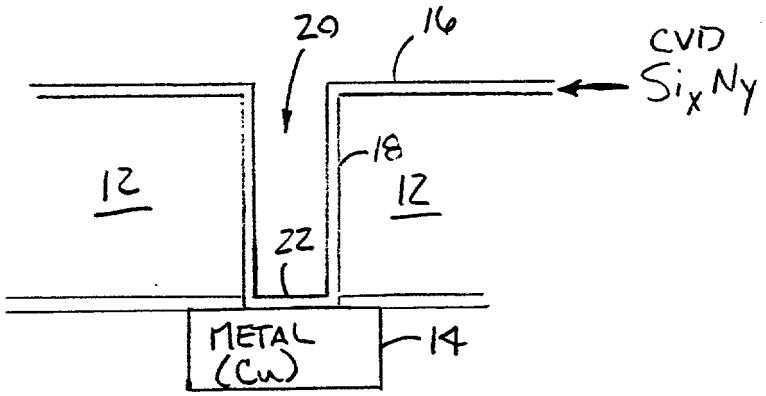

FIGURE 2

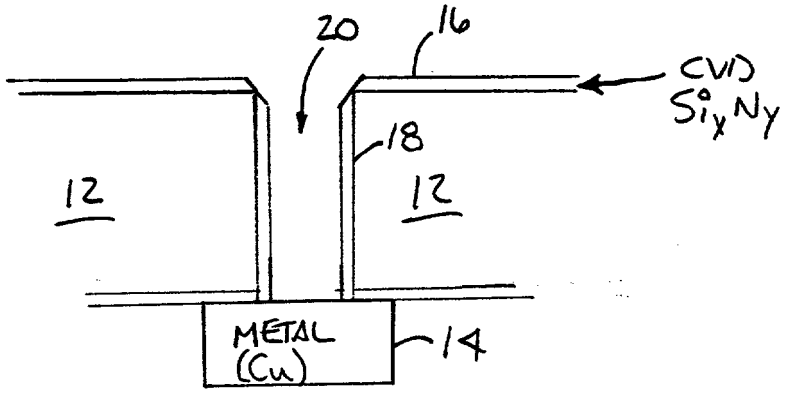

FIGURE 3

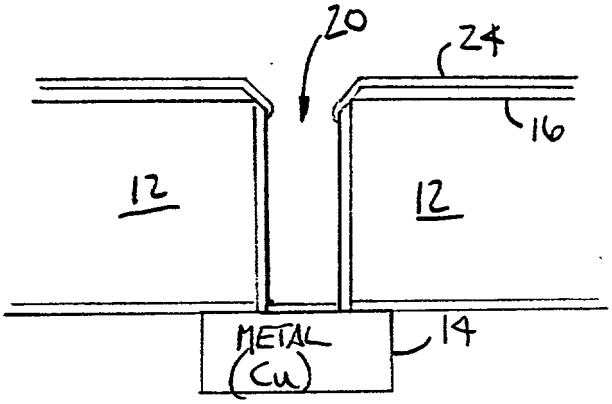

FIGURE 4

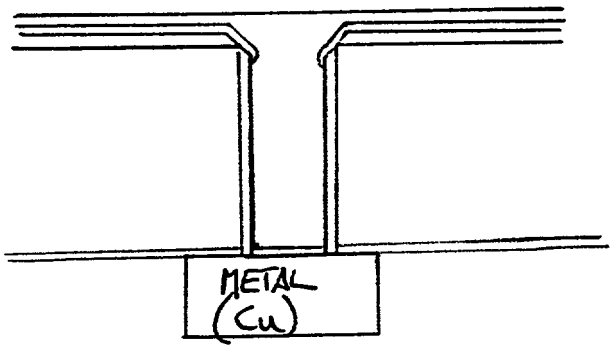

FIGURE 5

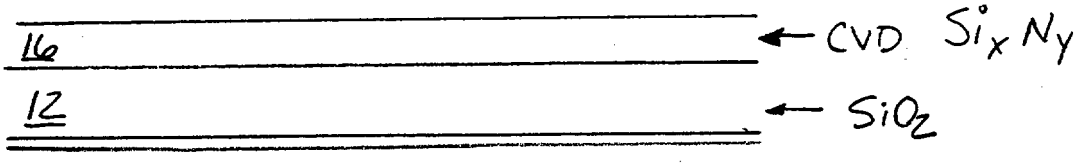

FIGURE 7

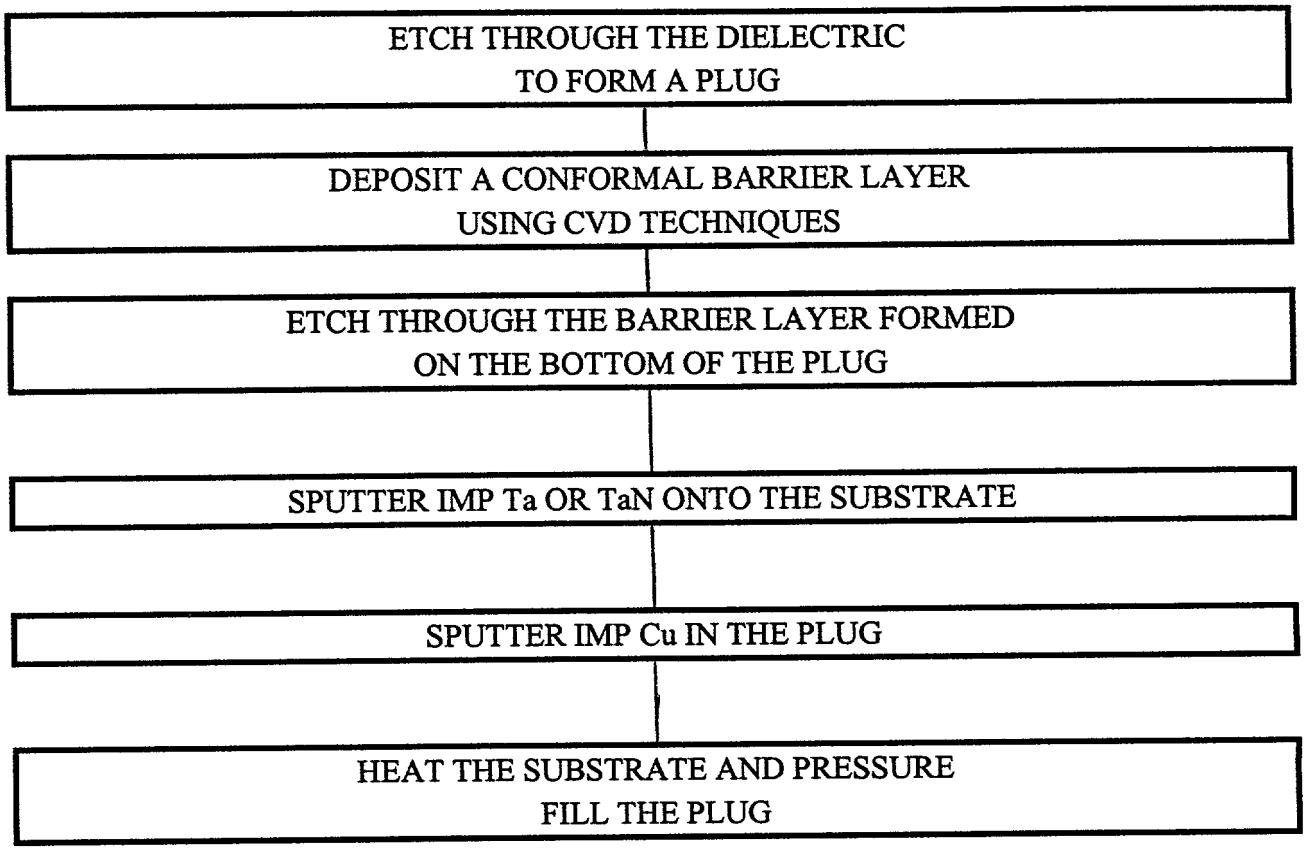
ETCH THROUGH THE DIELECTRIC
TO FORM A PLUG
DEPOSIT A CONFORMAL BARRIER LAYER
USING CVD TECHNIQUES
ETCH THROUGH THE BARRIER LAYER FORMED
ON THE BOTTOM OF THE PLUG
SPUTTER IMP Ta OR TaN ONTO THE SUBSTRATE
SPUTTER IMP Cu IN THE PLUG
HEAT THE SUBSTRATE AND PRESSURE
FILL THE PLUG

FIGURE 6

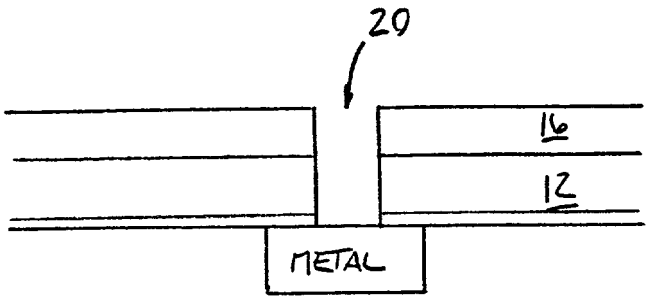

FIGURE 8

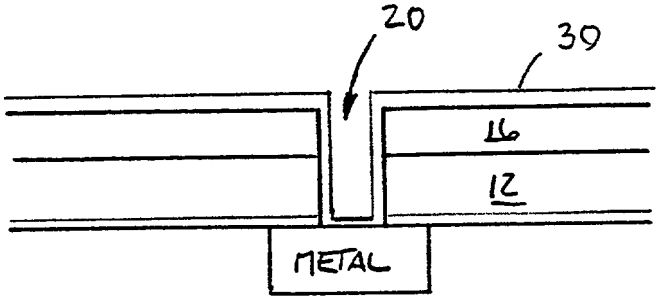

FIGURE 9

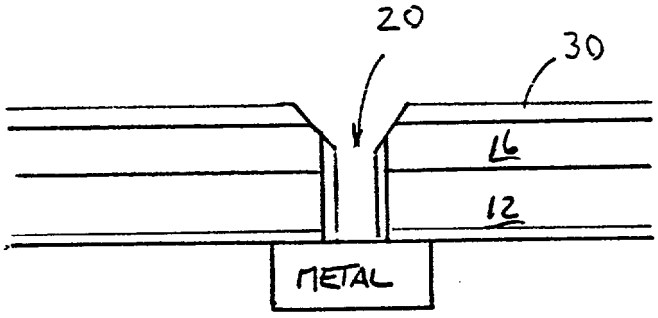

FIGURE 10

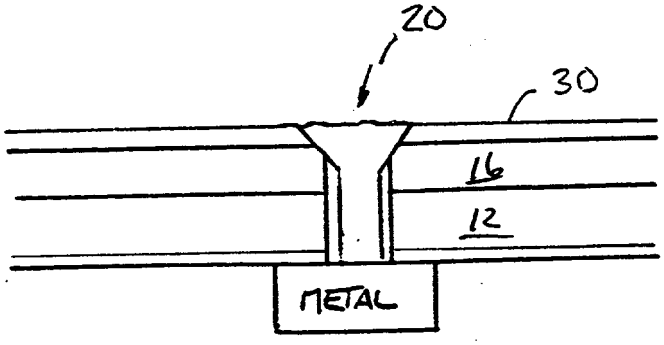

FIGURE 11

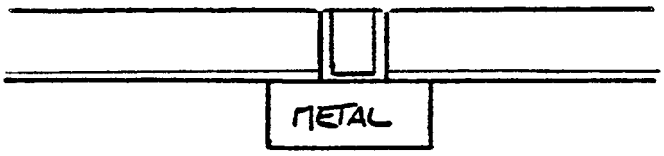

FIGURE 12

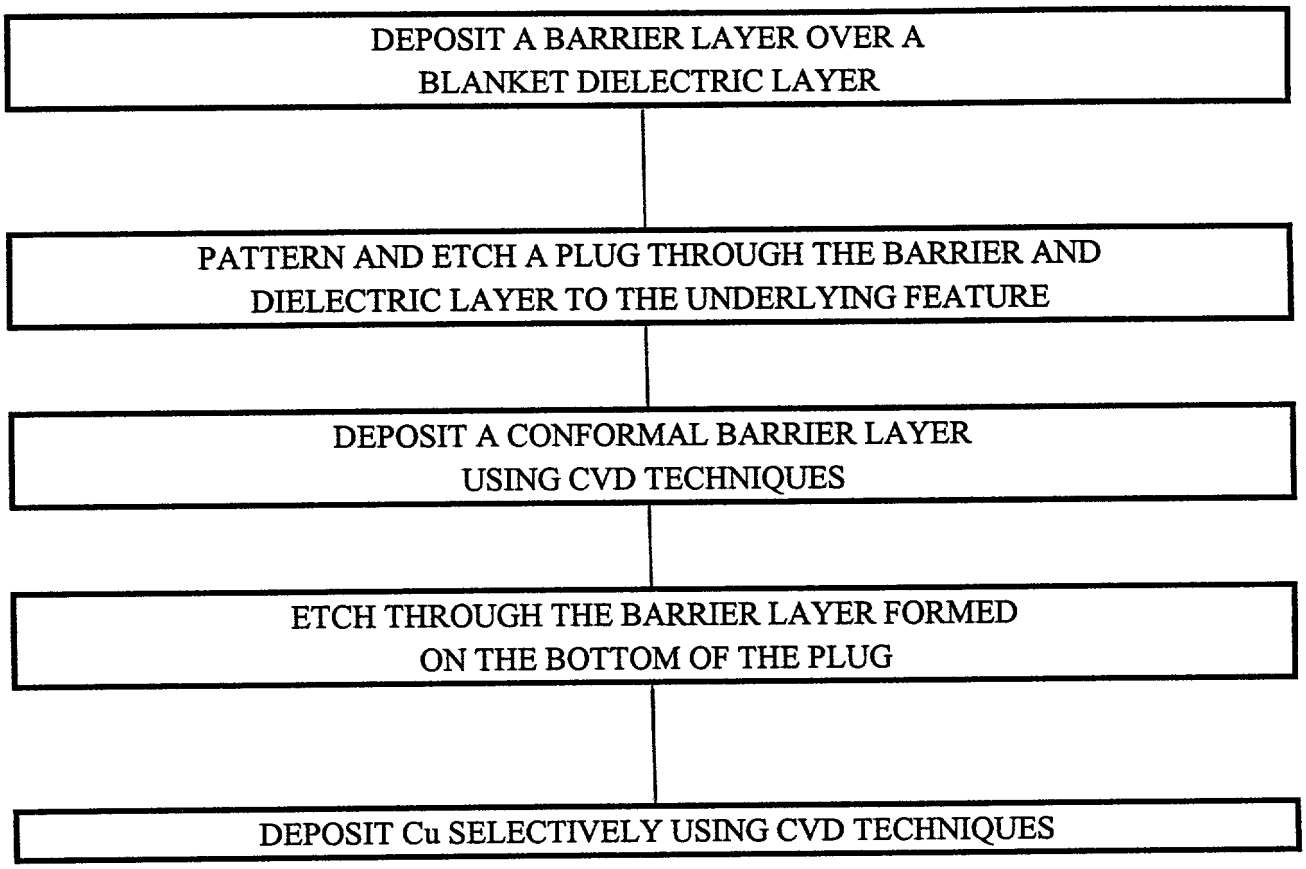
DEPOSIT A BARRIER LAYER OVER A BLANKET DIELECTRIC LAYER
PATTERN AND ETCH A PLUG THROUGH THE BARRIER AND DIELECTRIC LAYER TO THE UNDERLYING FEATURE
DEPOSIT A CONFORMAL BARRIER LAYER USING CVD TECHNIQUES
ETCH THROUGH THE BARRIER LAYER FORMED ON THE BOTTOM OF THE PLUG
DEPOSIT Cu SELECTIVELY USING CVD TECHNIQUES

FIGURE 13

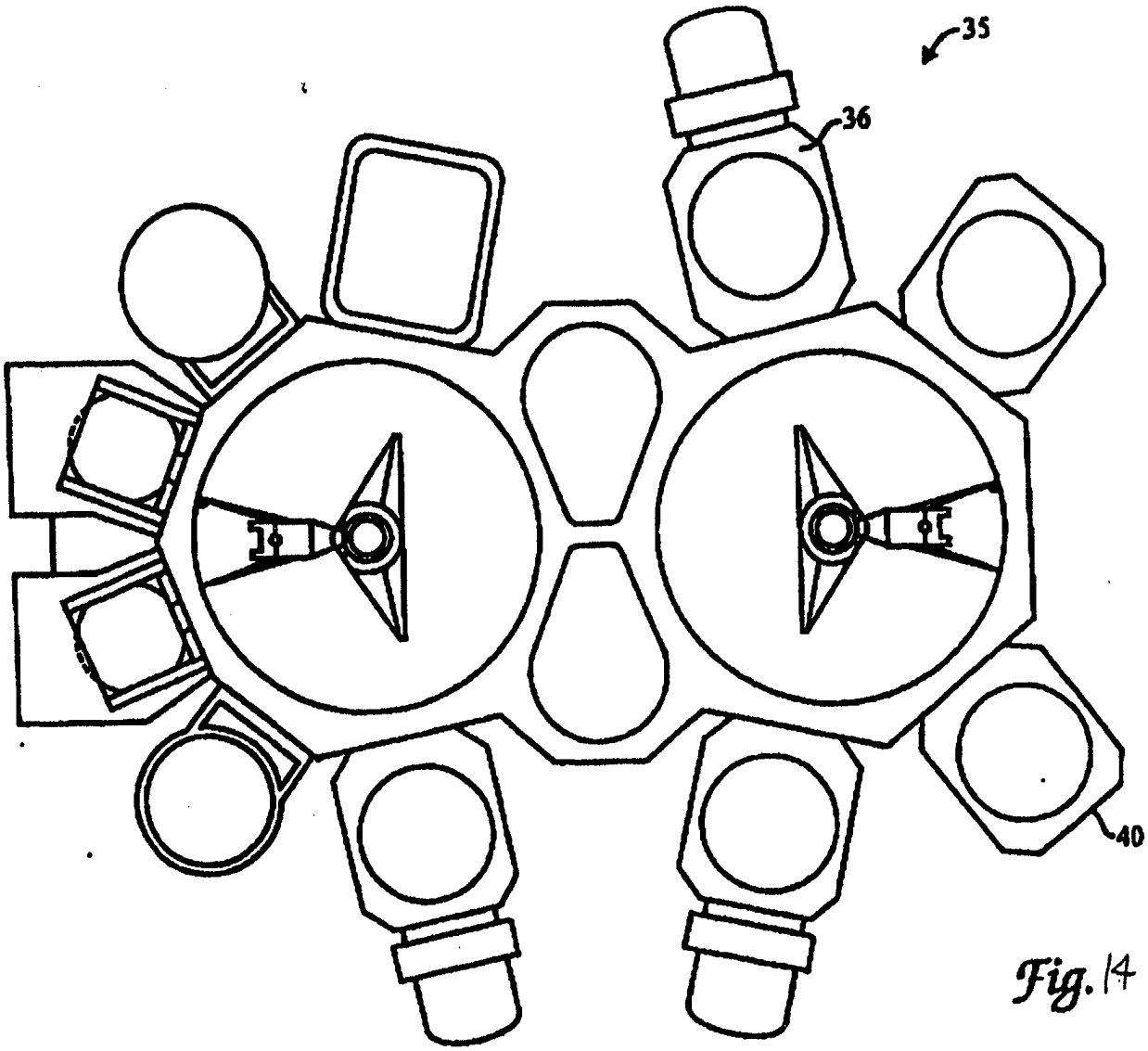

Fig. 14

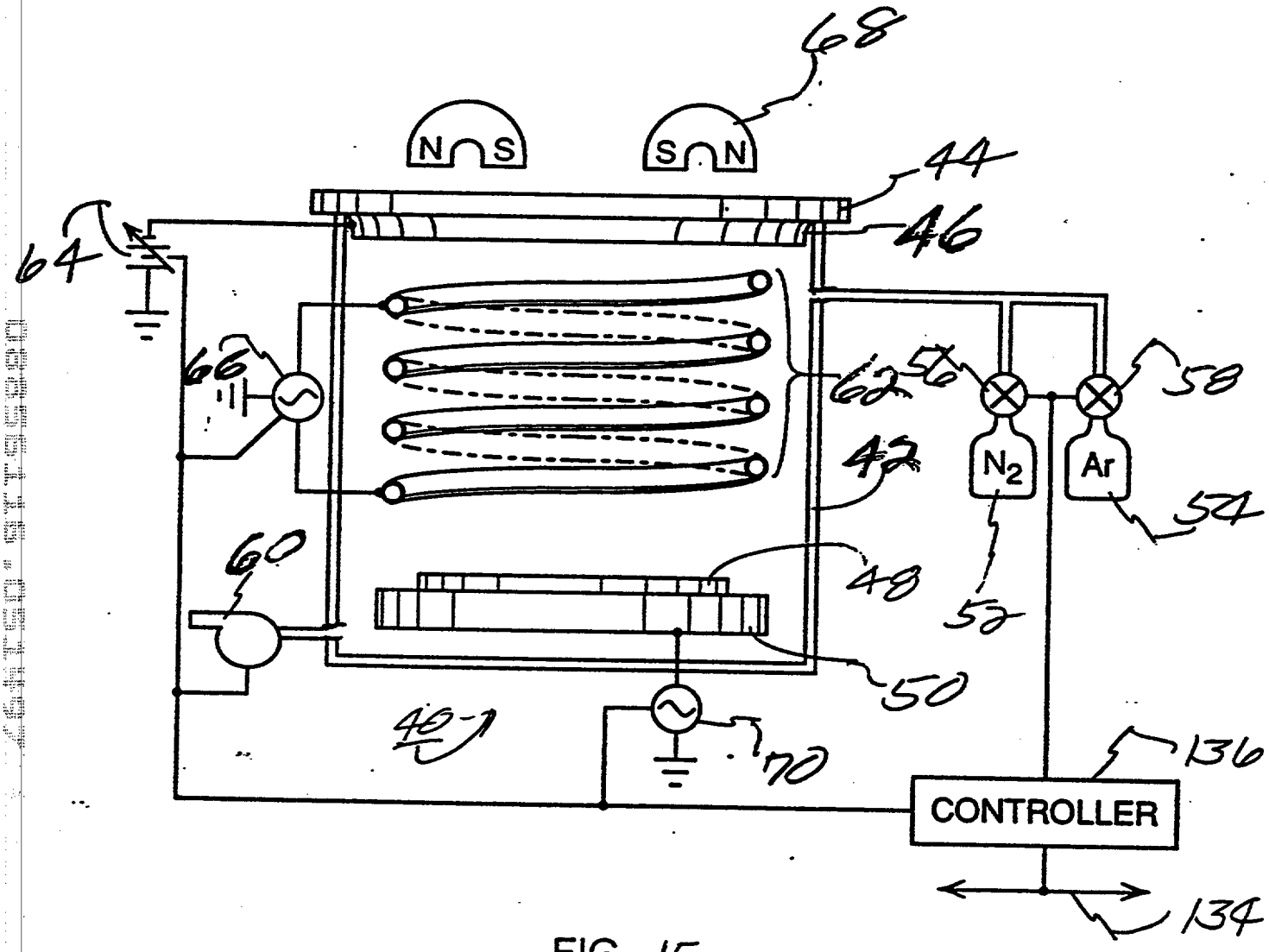
68
N S
S N
44
46
64
66
62
56
58
42
N_2
Ar
54
60
48
52
50
40
70
136
CONTROLLER
134

FIG. 15

Process Gas
RF Match Network
Plasma Generator Power Supply
Exhaust
40
50
55
65
20
95
75
80
70
105
110
45
127
115
116

Fig. 16

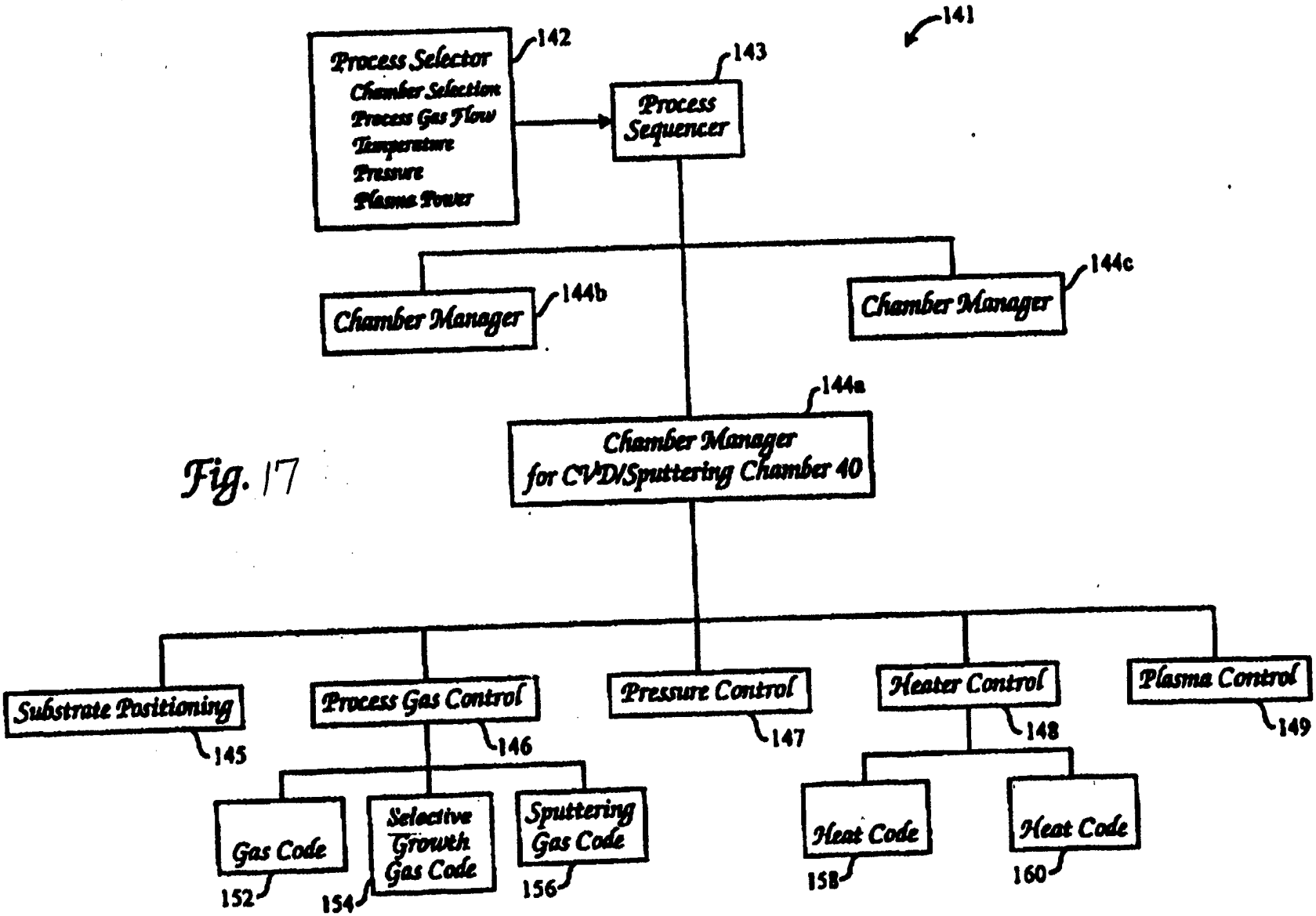
141
Process Selector
Chamber Selection
Process Gas Flow
Temperature
Pressure
Plasma Power
142
Process Sequencer
143
Chamber Manager
144b
Chamber Manager
144c
Chamber Manager for CVD/Sputtering Chamber 40
144a
Substrate Positioning
145
Process Gas Control
146
Pressure Control
147
Heater Control
148
Plasma Control
149
Gas Code
152
Selective Growth Gas Code
154
Sputtering Gas Code
156
Heat Code
158
Heat Code
160

Fig. 17

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

This declaration is of the following type:

[X] original
[ ] divisional
[ ] continuation
[ ] continuation-in-part

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

"RELIABILITY BARRIER INTEGRATION FOR CU APPLICATION"

SPECIFICATION IDENTIFICATION

The specification of which:

[X] filed herewith;
[ ] was filed on_____, under Serial No. _____, executed on even date herewith; or
[ ] Express Mail No. _____ (Serial No. not yet known)
and was amended on _____ (if applicable)
[ ] was described and claimed in PCT International Application No._____
filed on _____ and as amended under PCT Article 19 on _____.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56,

and which is material to the examination of this application; namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and

[ ] In compliance with this duty there is attached an Information Disclosure Statement in accordance with 37 CFR §1.98.

PRIORITY CLAIM (35 U.S.C. §119)

I hereby claim foreign priority benefits under Title 35, United States Code, §119, of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below, and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

[X] No such applications have been filed.

[ ] Such applications have been filed as follows:

A. Prior foreign/PCT application(s) filed within 12 mos. (6 mos. for design) prior to this application, and any priority claims under 35 U.S.C. §119

Country/PCT	Application No	Date Filed	Priority Claimed
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No

B. All foreign application(s), if any, filed more than 12 mos. (6 mos for design) prior to this U.S. application

Country:
Application No:
Filing date:

PRIOR CLAIM (35 U.S.C. §120)

I hereby claim the benefit under Title 35, United States Code, Section 120, of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information that is material to the examination of this application (namely, information where there is substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application.

[ ] No such applications have been filed
[ ] Such application have been filed, as follows:

		Status		
Serial No.	Filing Date	Patented	Pending	Abandoned
(None)				

POWER OF ATTORNEY

I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Sec. 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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Full name of **second** inventor: LIANG-YUH CHEN

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